35 “
” 2001 12 2002
“
”

IEEE/ACM CC2001 SWEBOK SE2004 CCSE2004

“ ”

4—5

IT 2002
IBM 40
“ 3+1 ”

1/2
4—6

SRTP

2007
2009 “ ”
“ ”

2018

.

.

1 +

2 UML

2

XML

3 +

. [redacted]

(1)

(4)

B07M0030	(A)I	4.5	96	4	0	0	6		2	+	
B07M0110	(A)( )I	4.5	96	4	0	0	6		2	+	
B07M0040	(A)II	5	96	4	0	0	6		3	+	
B07M0120	(A)( )II	5	96	4	0	0	6		3	+	
B07M0180	(B)	3	64	4	0	0	4		2	+	
B10M0030	(B1)I	3	64	0	0	0	4		3	+	
B10M0140	( )I	1	0	32	0	0	2		3	-	
B10M0040	(B1)II	3	48	0	0	16	3		2	+	
B10M0150	( )II	1	0	32	0	0	2		2	-	
B07M0210	(A)	2.5	48	4	0	0	3		3	+	
		23	416	80	0	16					

(5) ( )

B00TL010	(6)	6	96	0	0	0	0				
B00TL060	(2)	2	32	0	0	0	0				
B00TL070	(2)	2	32	0	0	0	0				
		10	160	0	0	0					

(6)

B7110010	( )	1	16	0	16	0	2		2	-	
B7110020	( )	1	16	0	16	0	2		2	-	
B7110030	( )	1	16	0	16	0	2		2	-	1
B7110040	( )	1	16	0	16	0	2		2	-	
		1	16	0	16	0					

(1)

B7110050	( )	2	32	32	16	0	4		2	+	
B7110060	1( )	2	32	24	0	0	3		3	+	
B7110070	( )	4	64	0	0	0	4		3	+	
B7110080	( )	4	64	16	0	0	4		2	+	
B7110090	2( )	2	32	32	8	0	2		2	+	
B7110100		4	64	16	0	0	4		2	+	
B7110110		2	32	0	0	0	2		3	+	
B7110120	( )	3	48	16	8	0	4		3	+	
B7110130	( )	3	48	16	16	0	4		2	+	
		26	416	152	48	0					

(2)

B7110150	UML( )	2	32	16	0	0	3		2	+	
B7110160	( )	2	32	0	0	0	2		2	+	
B7110170	( )	3	48	32	8	0	2		3	+	
B7110180		2	32	0	0	8	2		3	+	
B7110190		3	48	16	0	0	3		2	+	
B7110200		2	32	16	0	0	2		2	+	
B7110210		3	48	0	0	16	3		3	+	
		17	272	80	8	24					

(3)

B7110220	IT ( )	0.5	16	0	0	0	1		3	-	
B0493020		2	32	0	0	0	2		2	+	
B7110230	( )	2	32	0	0	0	2		2	+	
B0609010	VLSI ( )	2	32	0	0	0	2		3	+	6
B2204510	( )	2	28	8	0	0	2		3	+	
B7110240	( )	2	32	0	0	0	2		3	+	
B7110250		2	32	0	0	0	2		3	+	A
B7110260		2	32	0	0	0	2		2	-	
B7110270	( )	2	24	0	24	8	2		3	+	
B7110280		2	32	0	0	8	2		3	+	A
B7110310		2	32	4	12	0	2		3	+	
B7110300	( )	2	32	32	0	0	2		2	+	A
B7110320		2	32	0	0	0	2		3	+	
B7110340		2	32	0	0	0	2		2	+	A
B7110350	(/)	2	24	0	24	0	3		3	-	B
B7110360	XML (/)	2	24	0	24	0	3		3	-	
B7110370	(/)	2	24	0	24	0	2		2	-	
B7110390	(/)	2	24	0	24	0	3		2	-	
B7110380	(/)	2	24	0	24	0	3				B

&

	[redacted]										
B85M0010		1	0	0	0	0	(3)		1	-	

1

B85M0010		1	(3)	-		
	1					

2

B07M0030	(A)I	4.5	6	+		[4]
B07M0110	(A)( )I	4.5	6	+		
B07M0180	(B)	3	4	+		
B15M0030		3	3	+		
B15M0040		3	3	+		
B15M0060		2	2	-		
B15M0070	(1)	0.25	2	-		
B18M0010	I	0.5	2	-		
B7110050	( )	2	4	+		
B81M0030	1	0.5	(1)	-		
B17M0010	II	2	4	+		[1]
B17M0020	III	2	4	+		[2]
B17M0030	IV	2	4	+		[3]
B7110010	( )	1	2	-		
B7110020	( )	1	2	-		[6]
B7110030	( )	1	2	-		
B7110040	( )	1	2	-		[6]
	20.75					

3

B07M0040	(A)II	5	6	+		[5]
B07M0120	(A)( )II	5	6	+		
B10M0030	(B1)I	3	4	+		
B10M0140	( )I	1	2	-		
B15M0080	(2)	0.25	2	-		
B18M0020	II	0.5	2	-		
B7110060	1( )	2	3	+		
B7110070	( )	4	4	+		
B17M0020	III	2	4	+		[1]
B17M0030	IV	2	4	+		[2]
B17M0040	1	2	2	+		[3]
	17.75					

1

B7110500	1( )	2	(4)	-		
	2					

2

B10M0040	(B1)II	3	3	+		
B10M0150	( )II	1	2	-		
B15M0010		3	3	+		
B15M0090	(3)	0.25	2	-		
B18M0030	III	0.5	2	-		
B7110080	( )	4	4	+		
B7110090	2( )	2	2	+		
B7110100		4	4	+		
B7110150	UML( )	2	3	+		
B7110160	( )	2	2	+		
B17M0030	IV	2	4	+		[1]
B17M0040	1	2	2	+		[2]
B17M0050	2	2	2	+		[3]
	23.75					

3

B07M0210	(A)	2.5	3	+		
B15M0020		5	3	+		
B15M0100	(4)	0.25	2	-		
B18M0040	IV	0.5	2	-		
B7110110		2	2	+		
B7110120	( )	3	4	+		
B7110170	( )	3	2	+		
B7110180		2	2	+		
B7110240	( )	2	2	+		[9]
B7110250		2	2	+		
B7110310		2	2	+		[11]
B7110320		2	2	+		[12]
	18.25					

1

B7110510	2( )	2	(4)	-		
	2					

2

B15M0110	(5)	0.25	2	-		
B18M0050	V	0.5	0	-		
B7110130	( )	3	4	+		
B7110190		3	3	+		
B7110200		2	2	+		
B0493020		2	2	+		[7]
B7110230	( )	2	2	+		
B7110260		2	2	-		[9]
B7110300	( )	2	2	+		[11]
B7110340		2	2	+		[12]
B7110370	(/)	2	2	-		[14]
B7110390	(/)	2	3	-		
B7110440	(/)	2	3	-		[15]
B7110460	( )	2	3	-		[16]
B7110470	( )	2	3	-		[17]
	8.25					

3

B7110220	IT ( )	0.5	1	-		[8]
B15M0120	(6)	0.25	2	-		
B18M0050	V	0.5	0	-		
B7110210		3	3	+		
B7110520		2	3	-		
B7110530		1	1	-		
B88M0010		0.5	1	-		
B0609010	VLSI ( )	2	2	+		[7]
B2204510	( )	2	2	+		
B7110270	( )	2	2	+		[10]

1

0						

2
