



Secure boot, trusted boot and remote attestation for ARM TrustZone-based IoT Nodes

Zhen Ling^{a, <}, Huaiyu Yan^a, Xinhui Shao^a, Junzhou Luo^a, Yiling Xu^b, Bryan Pearson^c, Xinwen Fu^d

^a Southeast University, Nanjing, China

^b Alibaba Group, Hangzhou, China

^c University of Central Florida, Orlando, FL, USA

^d University of Massachusetts Lowell, Lowell, MA, USA

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ABSTRACT

With the extensive application of IoT techniques, IoT devices have become ubiquitous in daily lives. Meanwhile, attacks against IoT devices have emerged to compromise IoT devices by tampering with system pre-installed programs or injecting new malware. To mitigate these attacks, integrity enforcement of IoT systems has been proposed. The integrity of an IoT device system includes load-time integrity and runtime integrity. In this paper, we design an IoT system based on ARM TrustZone to enforce the system integrity. First, we establish the root of trust and propose a hybrid booting approach consisting of both secure boot and trusted boot to enforce the system load-time integrity. Second, we investigate a paging-based process integrity measurement method to measure the NW processes and conduct remote attestation based on the measurement results ensuring the NW runtime process integrity. We implement an IoT prototype system on a NXP i.MX6Q SABRE SD development board to assess its feasibility. Real-world experiment results demonstrate that our prototype introduces negligible performance overhead to the original system.

1. Introduction

The widespread usage of smart devices in various industries and fields brings a new era of Internet of Things (IoT). It is estimated that a total number of 11.7 billion IoT devices are actively connected to the Internet at the end of 2020, occupying 54% of overall online devices, and 30 billion IoT connections are expected by 2025 [1]. The global IoT market size has reached \$250 billion in 2019 and is predicted to reach \$1463 billion by 2027 [2]. However, despite of the rapid growth of IoT device number and market size, security has been overlooked due to the lagging IoT security standards, inadequate investment in security development as well as the lack of security awareness.

In recent years, extensive research efforts have been conducted to attacks against IoT devices, including hardware attacks, operating system (OS)/firmware attacks, and software attacks. (1) Hardware attack: For IoT devices deployed in public places, such as surveillance cameras, attackers can have physical access to them and leverage hardware interfaces like universal asynchronous receiver/transmitter (UART) and joint test action group (JTAG) interfaces to illegally tamper with the internal IoT system [3–5]. (2) OS/Firmware attack: The operating system

image or firmware are usually stored in flash memory for IoT devices and can be updated through network. The contents of a flash memory can be maliciously modified through hardware attacks and a malicious firmware image can be used for updating [6]. (3) Software attack: Software vulnerabilities of IoT devices, like stack overflow, command injection, etc. [7], can be leveraged to inject malware or maliciously modify existing programs. All of these attacks involve tampering with IoT system software, thus damaging the integrity of the original IoT system.

To mitigate such attacks and enforce system integrity, some research works have leveraged virtualization techniques to conduct system runtime execution monitoring (REM) [8,9]. These solutions rely on virtual machine monitors (VMM), namely hypervisors, that may contain vulnerabilities due to their large codebase, and can be maliciously modified before system boot. Meanwhile, the performance overhead introduced by the virtualization-based REM is intolerable for low-cost IoT devices.

Compared to x86 instruction set architecture, ARM, with virtues of energy efficiency, is more suitable for low-cost IoT devices and has

< Corresponding author.

E-mail addresses: zhenling@seu.edu.cn (Z. Ling), huaiyu_yan@seu.edu.cn (H. Yan), xinhuishao@seu.edu.cn (X. Shao), jluo@seu.edu.cn (J. Luo), yiling.xyl@alibaba-inc.com (Y. Xu), bpearson@knights.ucf.edu (B. Pearson), xinwen_fu@uml.edu (X. Fu).

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dominated the embedded system market, especially the mobile market [10]. Additionally, recent ARM processors provide a system-level security solution called TrustZone [11], which provides system-level isolation by dividing both system hardware and software resources into two domains, namely the Secure World (SW) and the Normal World (NW). The SW is more privileged and can be leveraged to conduct REM on the NW.

In order to enforce a strong system integrity policy, we leverage ARM TrustZone technology to ensure both the load-time integrity and the runtime integrity of the IoT system.

To enforce load-time integrity, we first establish the root of trust (RoT) based on the OCROM and eFuse. Then, we propose a hybrid booting approach consisting of the secure boot of the SW and the trusted boot of the NW. The secure boot involves establishing a chain of trust (CoT) initiated from the RoT for the SW boot images to ensure the SW load-time integrity, while the trusted boot involves measurements of the NW boot images and a remote attestation is conducted to verify the NW load-time integrity.

On such basis, we investigate a paging-based process integrity measurement and attestation method to monitor the NW status from SW. A periodical measurement is conducted inside the SW on the code segments of each NW process and the measurement results are sent to a remote attestation server. The NW runtime process integrity is verified if the received measurement results match with some pre-calculated reference values.

We implement a prototype system on a Freescale i.MX6Q SABRE SD development board [12] and evaluate its effectiveness against all these attacks. According to experimental results, our system introduces negligible performance overhead to the original IoT system.

In summary, our contributions in this paper are listed as follows:

- We propose a hybrid booting approach based on ARM TrustZone technology to enforce system load-time integrity.
- We investigate a paging-based process integrity measurement and attestation method to enforce runtime process integrity.
- We implement a prototype system on a Freescale i.MX6Q SABRE SD development board. Extensive empirical experiment results demonstrate that our system can effectively defend and detect different IoT attacks with little performance overhead.

The rest of this paper is organized as follows. Section 2 provides the necessary background information on TrustZone, secure boot and trusted boot. The system overview is presented in Section 3. The details of the hybrid booting approach and the paging-based process integrity measurement and attestation method are introduced in Sections 4 and 5, respectively. Section 6 evaluates the system effectiveness and performance overhead. Related work is reviewed in Section 8. Finally, we conclude this paper in Section 9.

2. Background

2.1. TrustZone overview

The ARM TrustZone technology [13] is a system-level security extension to the ARM architecture since ARMv6. TrustZone divides the system into two domains, Secure World (SW) and the Normal World (NW), and enforces strong isolation between these worlds in terms of both hardware and software resources.

TrustZone leverages dedicated hardware components to enforce hardware resource isolation. An additional processor bit, Non-Secure (NS) bit, indicates the current CPU state and is propagated through the Advanced eXtensible Interface (AXI) system bus to the peripherals and the memory. A peripheral can be configured as secure or non-secure using TrustZone Protection Controller (TZPC), and a secure peripheral can only be accessed by the SW when NS bit is cleared. Additionally, the physical memory is separated into two isolated parts, i.e., the secure memory and the non-secure memory, via TrustZone Address

Space Controller (TZASC). The secure memory can only be accessed by SW and any attempted access from NW is blocked, while the non-secure memory can be accessed from both worlds. The switch between these two worlds is accomplished via a Secure Monitor Call (SMC) instruction.

Based on the hardware isolation mechanism provided by TrustZone, both SW and NW run separated software suites, including different operating systems and user-level applications. Generally, a rich OS and client applications (CA) run in the NW while a secure OS and trusted applications (TA) run in the SW. Programs in the SW have full access to all system resources while programs in the NW can only access NW resources but not those belonging to the SW. Therefore, security critical tasks are often deployed inside the SW to be protected from an insecure NW.

2.2. Secure boot and trusted boot

Secure boot is a mechanism that establishes a Chain of Trust (CoT) on all system boot images. Secure boot relies on the public key cryptography to verify image signatures before their execution [14]. A pair of public and private key is generated for image signing and verification. The private key is used to sign an image offline while the public key is used to verify the image signature before one image is executed. The whole secure boot process usually involves several images. The image of the former boot stage verifies the image of the next boot stage, which in turn forms a verification chain, known as the CoT. During the secure boot, a single signature verification failure can terminate the whole system booting process.

As for trusted boot, all system boot images are measured in each boot stage [15]. The measurement results are accumulated to generate a measurement list which uniquely identifies the particular firmware images executed so far. The measurement list can be used for attestation. During trusted boot, an attestation failure will not terminate the system, but the user may be alerted via a smart app.

Both secure boot and trusted boot anchor their trust on a root of trust (RoT), which is inherently trusted. Therefore, the RoT is usually established based on some invariable storage media whose content cannot be modified once programmed.

3. System overview

In this section, we present the threat model and the basic idea of the system design.

3.1. Threat model

We assume that attackers have physical access to IoT devices. They can launch hardware attacks [3–5], OS/firmware attacks [6] and software attacks [7] against IoT devices. Before the IoT devices are powered up, the attackers can tamper with the firmware images of both the SW and the NW stored in the flash memory. During system runtime, the attackers can inject malware in the NW and tamper with NW built-in programs arbitrarily. Sophisticated hardware attacks like bus snooping attacks [16], cold boot attacks [17] and cache side channel attacks [18] are out of the scope of this paper. We only consider the security of the code section of a program, i.e., *text*.

We assume that the program in ROM is secure since the On-Chip ROM (OCROM) is read-only and difficult to tamper with. We also assume that the attackers cannot compromise the run-time SW; therefore, SW code is secure from software attacks. Finally, we assume that the remote attestation server is secure and trustworthy.

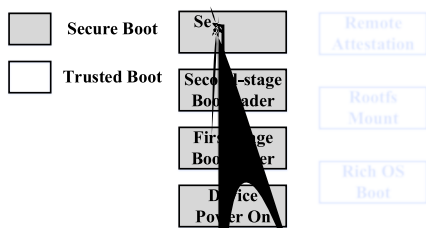


Fig. 1. The hybrid booting sequence.

3.2. System design

We propose a hybrid secure and trust booting method and a process integrity measurement and attestation method to ensure the system load-time integrity and run-time process integrity, respectively.

The hybrid booting procedure is comprised of the secure boot of the SW and the trusted boot of the NW. Fig. 1 illustrates the hybrid booting sequence. On powering up, the first-stage bootloader starts to run first. It loads the second-stage bootloader into memory, verifies its integrity

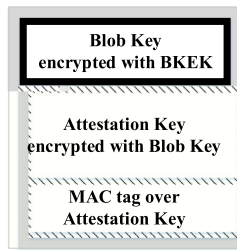


Fig. 3. CAAM blob structure.

4.3. Trusted boot

After the secure OS kernel gets started, trusted boot is used to boot up the NW to ensure its integrity. The trusted boot for the NW involves two phases: the offline hash chain calculation phase, and the online trusted boot phase. Furthermore, the remote attestation key needs to be securely stored in the flash memory.

4.3.1. Offline phase

We design a hash chain to measure the NW images, as shown in the upper half of Fig. 4. The initial hash value is set to 0 ($V = 0$). The hash value is updated by concatenating the current value V and next image I on the chain, $V = Hash.VBI$. The NW consists of two images: the rich OS kernel image and the file system image. Therefore, the final value of the hash chain is calculated as $V = Hash.Hash.0BI_1/BI_2$ and it is stored in the remote attestation server as the reference value for NW integrity verification.

The final hash value V is encrypted with the remote attestation key before being sent to the remote attestation server for NW integrity verification. The remote attestation key is a symmetric encryption key and is generated offline. Both the remote attestation server and the IoT

4096 Bytes
...
4096 Bytes
2116
...

Fig. 6. Measurement results of the *init* code segment.

5. Paging-based process integrity measurement and attestation method

In this section, we present the basic idea of process integrity measurement. Then we elaborate on the process integrity measurement method and the process integrity remote attestation method.

5.1. Basic idea

We propose a paging-based process integrity measurement and attestation method to ensure the integrity of NW processes at the runtime. Recall that the SW is trusted at the load-time and runtime as the secure boot of the SW and TrustZone hardware isolation techniques are applied. However, NW programs are still untrusted at the runtime despite of the NW trusted boot, since the NW may be invaded by attackers who can inject malware or tamper with built-in programs in the NW. Note that, different from PC environment, after an IoT device is deployed, the system always executes the same set of pre-installed programs instead of installing new programs on user demand. As a result, we can perform offline measurement on the code sections of the pre-installed programs at the page granularity level in the NW and store measurement results as reference values on the remote attestation server. Then we measure the code segments of the runtime processes residing on the memory page using a measurement TA in the SW, and finally send the results to the remote attestation server to verify the integrity of processes.

5.2. Offline program measurement

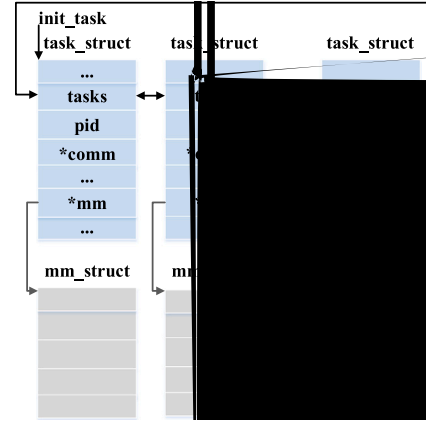
All of the program code are stored in the *.text* section of the corresponding ELF files of the programs. However, the code is loaded and run in the memory in terms of the paging mechanism. Therefore, the *.text* sections of all NW programs can be divided into several segments in terms of a page size (i.e., 4 KB) offline. The hash values of each segment are calculated and saved on the attestation server as the reference values to verify the integrity of NW processes.

We take the first user-level process (i.e., *init*) as an example. The size of its code segment is of 0x6844 bytes, occupying 7 pages in terms of a 4 KB page size. The last part that cannot occupy one full page is handled in accordance with its actual size. A SHA256 hash of each page is calculated, generating 7 structures of *^processname, pagehash^*, as shown in Fig. 6. The *^processname, pagehash^* structures of all NW ELF files are calculated and saved in a hash table on the attestation server as the reference for process integrity verification.

5.3. Runtime process integrity measurement

The SW measurement TA measures the code segment of each process periodically in the memory. After encrypting the measurement results with the remote attestation key, the measurement TA sends them to the attestation server that verifies the runtime process integrity.

In Linux, processes are managed using the process descriptor *task_struct* shown in Fig. 7. Each *task_struct* manages one process and contains all information of that process, including process ID,

Fig. 7. Linux *task_struct* and *mm_struct*.

process name, address space, etc. All *task_struct*s are organized as a doubly-linked list by the field *tasks*. The virtual address of process 0's *task_struct*, named *init_task*, is stored in the kernel symbol table file, i.e., *System.map*. Starting from *init_task*, all *task_struct*s can be traversed and the information of all processes can be collected. The field *mm* of *task_struct* points to a memory descriptor *mm_struct* which is used to manage the virtual address space of a process. The fields *start_code* and *end_code* describe the starting and ending address of the process code segment respectively and can be used to locate the code segment of a process in the memory.

Since the SW and NW have different virtual memory address spaces, the NW virtual addresses should be translated into physical addresses. Then these physical addresses are mapped to SW virtual addresses. Linux divides a process' virtual address space into two parts, i.e., the kernel space and the user space. The kernel space uses the linear address translation method. There is a fixed interval *va2pa_offset* between a kernel space virtual address *va_kernel* and its corresponding physical address *pa_kernel*, as shown in Eq. (1).

$$pa_kernel = va_kernel * va2pa_offset \quad (1)$$

The user space conducts address translation using paging. The field *pgd* of *mm_struct* points to the base address of the page table. A user space virtual address *va_user* can be translated to its corresponding physical address *pa_user* through page table walk *page_table_walk*, as shown in Eq. (2).

$$pa_user = page_table_walk.pgd, va_user/ \quad (2)$$

The secure OS uses one-level paging structure to manage the SW memory space. A physical address *pa* is mapped into the SW virtual address space using Eq. (3).

$$va = page_table.pa/ \quad (3)$$

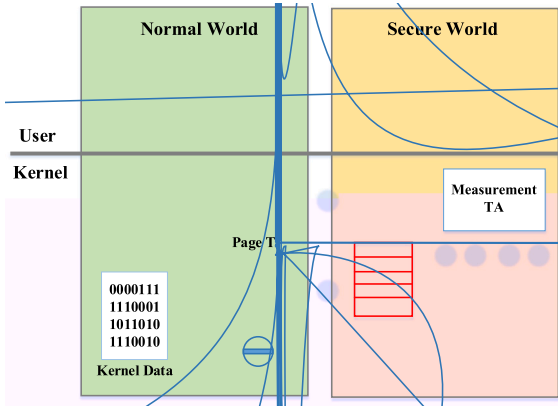


Fig. 8. Measuring pages of NW process code segments.

- (1) The measurement TA maps the physical address of *init*'s *task_struct* into the SW virtual address space using Eq. (3) and obtains the *mm* field in accordance with the structure of *task_struct*. Note that the obtained *mm* contains the NW virtual address of *init*'s *mm_struct*.
- (2) The measurement TA obtains the physical address of *init*'s *mm_struct* according to Eq. (1).
- (3) The physical address of *init*'s *mm_struct* is transformed to the corresponding SW virtual address according to Eq. (3). The measurement TA obtains *start_code*, *end_code*, and *pgd* from *mm_struct*. Note that the obtained pointers also contain NW virtual addresses.
- (4) According to *start_code* and *end_code* as well as the page size, the measurement TA calculates the number of pages the *init* process's code segment occupies and the starting NW virtual address of each page. The physical address of *init*'s page table can be located using *pgd*. Since the code segment of *init* is in the NW user space, the virtual address of each page is transformed to its corresponding physical address according to Eq. (2). Besides, the measurement TA determines whether a page currently resides in the physical memory according to the *Present* bit of its corresponding page table entry.
- (5) The physical address of each page is transformed to the corresponding SW virtual address according to Eq. (3) and the measurement TA reads and measures the content of each page.

The SHA256 hash values of pages in the memory are calculated and concatenated to form a measurement result M of one process. The format of the result M is “##process name##number of page hashes##page hash 1, page hash 2, page hash 3, ..., page hash n ”.

5.4. Process integrity attestation

The NW process measurement results generated by the SW measurement TA are used as the attestation information and forwarded to the remote verifier by the NW attestation CA for NW process integrity remote attestation, as shown in Fig. 9. We design a protocol for the remote attestation. The detailed workflow is illustrated as follows.

- (1) The IoT device requests a *Nonce* from the remote verifier. After establishing a TLS connection to the remote verifier, the NW attestation CA requests a *Nonce* from the verifier and passes it to the SW measurement TA. The measurement TA makes a secure copy of the *Nonce* in the SW memory.
- (2) The measurement TA reads the memory pages of the i th NW process' code segment and calculates its measurement M_i .

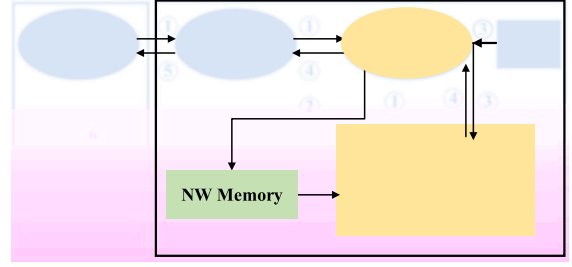


Fig. 9. NW process integrity remote attestation.

- (3) The measurement TA encrypts the attestation information. M_i and *Nonce* are encrypted with the remote attestation key K used in the trusted boot phase. Then we can obtain the ciphertext $E_i = AES * 128 * CBC.Nonce \parallel M_i, K$.
- (4) The measurement TA passes the ciphertext E_i to the attestation CA. The measurement TA obtains

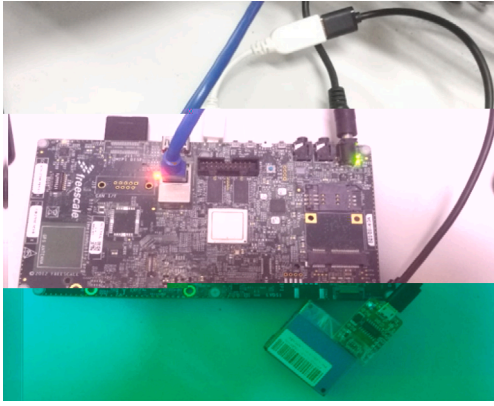


Fig. 10. Trusted air quality monitoring prototype.

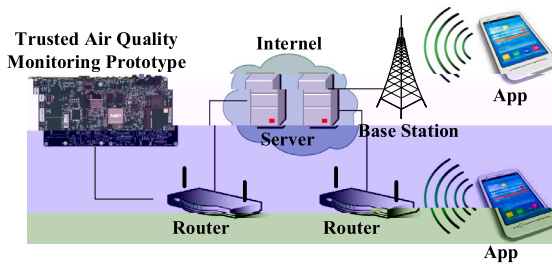


Fig. 11. Air quality monitoring prototype architecture.

6.2. Effectiveness

The evaluation of the secure boot process in the SW is aimed to verify whether the second-stage bootloader can detect any violation if the image of the secure OS, the public key, or the signature is tampered with. In the experiments, four different secure OS images are evaluated: an intact one, one with a tampered secure OS, one with a tampered public key, and one with a tampered signature. Only the intact image can boot successfully, while the others fail to boot up due to verification errors. The results show that the secure boot can enforce the load-time integrity of the SW.

The evaluation of the trusted boot process in the NW is aimed to verify whether our prototype can report the abnormal system status to the attestation server if the rich OS or the filesystem image is tampered with. After we tamper with the rich OS or the filesystem image, our prototype can boot up and function normally without being shut down by force. However, the remote attestation server has already detected the abnormal system status which can be sent to the user informing that the device is not trusted any more. The results show that by use of the trusted boot in the NW, even if NW images are tampered with, the NW programs can be executed, while the abnormal system status can be verified by the remote attestation server.

We assess the runtime process integrity measurement and attestation so as to verify whether our prototype can detect a newly-inserted malware or a tampered pre-installed program in the NW. We insert a malware into the NW. After the malware starts, the attestation server detects the malware and shows its name. Furthermore, we tamper with the code segment of a pre-installed program *serial_arm* in the NW. After restarting *serial_arm*, the attestation server indicates that a pre-installed program is tampered with. The results show that the paging-based process integrity measurement and attestation method can enforce runtime process integrity of the NW.

6.3. Performance

The performance evaluation of the hybrid boot is designed to measure the consumed time during the secure boot and trusted boot. We record the time consumed by both the secure boot module and the trusted boot module as well as the total booting time of second-stage bootloader and the secure OS, respectively. We conduct the timing measurement of the hybrid booting process for 30 times and take the average of the time. As the results shown in Table 1, the secure boot module introduces little overhead in the second-stage bootloader. Also, the trusted boot module slows down the secure OS booting process dramatically. The reason is that the filesystem image has a total size of 107 MB, and it takes a lot of time measuring it. Under real circumstances, the filesystem image can be compressed down to less than 1 MB, which can erase such performance bottleneck. In addition, a total booting time of approximate 9.2 s is tolerable in terms of user experience.

We evaluate the performance overhead introduced by the measurement TA and attestation CA in the paging-based process integrity measurement and attestation method. We use LMBench [19] to evaluate the system performance. In the experiments, we measure and compare the execution time of various Linux system services with the measurement TA and attestation CA enabled and disabled. We continuously call each system service for 1000 times, the call interval of each system service is 250 ms, and the whole performance evaluation lasts about 30 min. As shown in Table 2, when the measurement TA and attestation CA are enabled, the delay introduced to the evaluated services fluctuates between $\sim 0.55\%$ and $\sim 0.67\%$. The results show that our the measurement TA and attestation CA introduce negligible performance overhead to the original system, and it is feasible to actually deploy our prototype system. Note that the time interval of NW process integrity measurement event is determined based on the trade-off between performance and security. Due to the limited computing resources of IoT devices, frequent measurement events will jeopardize the whole system performance. Additionally, a period adaptation way can be taken to actively adjust the measurement time interval at the runtime [20].

7. Security analysis and limitations

This section conducts security analysis on both the hybrid booting approach and the paging-based process integrity measurement and attestation method and discusses their limitations.

7.1. The hybrid booting approach

The hybrid booting approach ensures that the system starts from a legal state. The root of trust in our hybrid booting approach is established based on the eFuse and OCROM which are tamper-proof. Starting from the RoT, a chain of trust is established through the secure boot phase and a single image verification failure will terminate the whole booting process. After a successful secure boot, the SW measures the NW images and the measurement results are used for remote attestation. If the NW images are maliciously modified by an attacker, the remote attestation will fail and the user is alerted. Therefore, any offline modification to both the SW and the NW images will be detected and the system can only be in normal operation after a successful hybrid boot.

7.2. The paging-based process integrity measurement and attestation method

Both the SW measurement TA and the measurement results are secure from the NW. The secure boot ensures that only pre-installed SW programs will run inside the SW. Base on the hardware isolation mechanism provided by TrustZone, the SW measurement TA cannot be compromised by the NW. Additionally, the measurement results are

Table 1
Results of hybrid boot performance evaluation.

	Secure/trusted boot module booting time (ms)	Total booting time (ms)	Ratio (–)
Second-stage bootloader	23.7	6430.0	0.37
Secure OS	1276.0	2863.0	44.57

Table 2
Results of LMBench performance evaluation.

System service	Program integrity measurement and data transfer OFF (s)	Program Integrity Measurement and Data Transfer ON (s)	Difference (–)
null syscall	0.4230	0.4253	+0.54
open/close	10.1292	10.1865	+0.57
pagefault	1.2594	1.2678	+0.67
signal handler install	1.1063	1.1082	+0.17
fork+exit	1159.5902	1153.2701	*0.55
fork+exec	3410.6390	3405.9838	*0.14
select(250fd)	16.4555	16.4623	+0.04

encrypted inside the SW and then forwarded to the NW for network transmission. Only the SW and the remote attestation server have access to the decryption key and the NW can never get the plaintext.

Our measurement method now relies on the integrity of NW Linux paging structure and process management kernel objects, i.e., *task_structs*. Therefore, our method is vulnerable to malware capable of self-hiding, for example, transient rootkits [21]. Meanwhile, the semantic gap issue involved in all REM projects is still an open research topic [22] and existing TrustZone-based approaches can provide security protection for such kernel objects [16,23]. We plan to dedicate these semantic invariant protection topics to our future work.

8. Related work

8.1. Research and application of TrustZone

TrustZone is researched and widely deployed on different computing devices, including mobile devices and IoT devices. (1) Mobile Devices. Most ARM-based mobile devices are protected by TrustZone-based TEE, such as smart phones produced by Apple, Samsung [24], Huawei [25], Xiaomi, etc. (2) IoT Devices. TrustZone is used to protect IoT smart devices. For example, Ukil et al. [26] proposed to provide data security for IoT devices based on the TrustZone isolation mechanism. TrustShadow [27] leverages TrustZone to protect programs from untrusted Rich OSes. The program is placed in the SW to be isolated from the Rich OS. Its requests for OS services are forwarded to the Rich OS and the returning results are verified by TrustShadow. Recently, TrustZone is leveraged to realize real-time communication for hybrid dual-OS systems [28].

8.2. System load-time integrity verification

System load-time integrity verification techniques, e.g., secure boot and trusted boot, are employed to defend offline firmware tampering attacks. Both secure boot and trusted boot require offline system integrity measurement before system usage [29] and verify each component step by step from the root of trust forming a chain of trust.

The hardware-based RoT has the virtues of stability, reliability and small attack surfaces and therefore is preferred over the software-based ones [15]. For example, NXP's i.MX 6 series applications processors implement High Assurance Boot (HAB) with boot ROM and eFuse as the RoT [30]. Trusted Platform Module (TPM) [31], Mobile Trusted Module (MTM) [32], Battery Backup Random Access Memory (BBRAM) [33] can be leveraged to implement hardware-based RoTs. The fingerprint of on-chip Static Random Access Memory (SRAM) can be used to restore the seed for device key generation and thus provide RoT for TrustZone SW [34].

8.3. System runtime integrity verification

System runtime integrity verification is widely deployed to detect malicious or abnormal behaviors in computer systems, such as malware injection and modification of pre-installed programs. For instance, DRIVE [35] verifies the integrity of processes by comparing the memory image of the process with the corresponding executable binary image. Chang et al. [9] propose a page-based process integrity verification method by measuring the pages of one executable program's code segment in a virtual machine. Upon each page fault triggered by demand paging, the missing page is measured and its integrity is verified before it is loaded into memory. Wang et al. [36] propose a data integrity detection method based on edge computing [37] where self-balancing binary search trees are leveraged to accelerate the data auditing process in the cloud. Recently, machine learning technologies have been leveraged to detect malware [38] and software vulnerabilities [39].

Hardware-based process integrity measurement and attestation have been widely researched. For example, Hristozov et al. [40] propose a Device Identity Composition Engine (DICE)-based system runtime integrity verification method for lightweight MCU-powered IoT devices. Wang et al. [41] propose a hardware-based Instruction Stream Integrity Checker (ISIC) to measure the integrity of instruction blocks during program execution. Wehbe et al. [42] propose to connect a target embedded device to an external hardware monitor. The hardware monitor is responsible for measuring the pages of the target system's processes and comparing the measurement results with the pre-calculated ones stored in its secure storage.

9. Conclusion

This paper designs a hybrid booting approach consisting of both secure boot and trusted boot to enforce the IoT system load-time integrity. On this basis, the paging-based runtime process integrity measurement and attestation method is designed and implemented. The trusted SW measures and verifies process integrity of the NW to enforce the runtime process integrity of the system. An IoT prototype system is implemented on an IMX6Q SABRE SD development board. Extensive evaluations are performed to demonstrate the effectiveness of the system.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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